REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

The specification has been amended to include headings and the abstract has been amended to be in a more traditional U.S. format. The claims have also been amended to be in a more traditional U.S. format. These amendments are not made for reasons relating to patentability.

Claims 1, 2 and 7-9 were rejected under 35 U.S.C. Section 102(b) as allegedly being "anticipated" by the Zeng publication.

Applicant traverses this rejection.

The office action refers to Figure 6 of Zeng which shows four storage elements which have been designated with hand-written notations as FF_1, FF_2, FF_3 and FF_5. There is a single EXOR gate that nominally connects the storage element designated as FF_1 with the storage element designated as FF_5.

In contrast thereto, claim 1 requires that a plurality of EXOR gates is provided ("...outputs and inputs of the storage elements are recursively interconnected with EXOR gates inserted ...") and for this reason Zeng cannot anticipate claim 1 or its dependent claims 2 and 7-9. Because a plurality of EXOR gates recursively interconnects the storage elements of the code-producing series, it is possible to systematically use several storage elements as target points for recursive connections in the code-producing series.

Further, this makes it possible to simultaneously use a plurality of different feed-back distances which of course is not possible with only a single EXOR gate.

Because the claim 1 code generator comprises a plurality of EXOR gates, wherein at least one of these EXOR gates is connected in the manner described in the "characterising" clause, it is possible to generate a code that is resistant to attack. In particular, the claim 1 code generator is resistant to the linear consistency attack, the linear syndrome attack and the Siegenthaler correlation attack mentioned in the Zeng publication. In this connection, one non-limiting, example embodiment includes a plurality of EXOR gates whose first inputs are connected with outputs of consecutively arranged storage elements. This feature is incorporated in new claim 10 which finds support, inter alia, in Figure 2 and the accompanying description in which consecutively arranged storage elements FF_2, FF_3, FF_4 and FF_5 are recursively interconnected by EXOR gates $EXOR_{p1}$, $EXOR_{p2}$, $EXOR_{p3}$ and $EXOR_{p4}$.

New independent claim 11 has been added. The subject matter of this claim finds support in the original disclosure (see, e.g., Figure 2). Zeng does not show two or more EXOR gates arranged in the manner recited in claim 11 and thus this claim patentably distinguishes from Zeng. Claims 12-18 refer to claim 11 and patentably distinguish from Zeng because of their respective dependencies and because of the additional patentable features recited therein.

New independent claim 19 recites a code generator comprising storage elements arranged in a code-producing series in which an output of a last storage element in the

series is coupled to an input of a first storage element in the series, and two or more logic gates. The logic gates include an EXOR and an EXNOR gate, each of which includes first and second inputs respectively coupled to outputs of first and second corresponding storage elements and an output coupled to an input of a third corresponding storage element. This claim finds support in the Figures and the description (see, e.g., page 3, lines 26-30). Zeng does not disclose or suggest a code generator including an EXOR and an EXNOR gate arranged as recited in claim 19 and thus this claim and its dependent claim 20 patentably distinguish from Zeng.

The pending claims are believed to patentably distinguish over the applied references and favorable office action is respectfully requested.

Respectfully submitted,

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